EXHIBIT 026

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
1. Integrated circuit comprising a plurality of processing modules (M, S) said modules being disposed on the same chip, and	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Lenovo IdeaPad Duet 3 Chromebook (hereinafter, the "Lenovo product") includes an integrated circuit. For example, the Lenovo product includes the Qualcomm Snapdragon 7c Gen 2 Compute Platform system on chip (hereinafter, the "Snapdragon SoC").  **Lenovo IdeaPad Duet 3 Chromebook** Featuring a Snapdragon 7c Gen 2 Compute Platform The Lenovo IdeaPad™ Duet 3 Chromebook is the ideal work and play device for the hyper-mobile user looking for superior experience with the larger 11" 2K near-borderless display. Faster connectivity options, all-day battery life, and the more powerful, fanless and efficient performance of the Snapdragon® 7c Gen 2 platform gets things done while on the go. Work on the detachable keyboard or take notes and sketch with the optional Lenovo USI Pen 2. 1 2 3 4 Learn More https://www.qualcomm.com/products/application/mobile-computing/laptop-device-finder/lenovo-ideapad-duet-3-chromebook

[1] The Lenovo product is charted as a representative product made used, sold, offered for sale, and/or imported by Lenovo. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein

U.S. Patent No. 7,366,818 (Radulescu & Goossens)

"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	The Snapdragon SoC comprises a plurality of processing modules, for example Qualcomm Adreno GPU; Octa-core Qualcomm Kryo 468 CPU; and Qualcomm Hexagon 692 DSP:

Qualcomm® Snapdragon™

7c Gen 2 Compute Platform

Qualcomm snapdragon

Specifications & Features

CPU

- CPU Clock Speed: Up to 2.55 GHz
- CPU Cores: Octa-core Qualcomm® Kryo™ 468 CPU
- CPU Architecture: 64-bit

Process

- Process Technology: 8 nm

OS Support

- Supports Windows 10 and Windows 11
- Chrome OS

Memory

- Memory Type: 2 x 16-bit, LPDDR4x-4266

Storage

- UFS: eMMC 5.1; UFS 2.1

Visual Subsystem

- GPU: Qualcomm® Adreno™ GPU

Camera

- Image Signal Processor: Qualcomm Spectra™ 255 image signal processor, 14-bit
- Dual Camera, ZSL, 30fps: Up to 16 MP

Video

- Video Playback: Up to 4K HDR10
- Codec Support: H.265 (HEVC), H.264 (AVC), VP9
- Video Software: Motion Compensated Temporal Filtering (MCTF)

Display

- Max On-Device Display: QXGA @ 60Hz, FHD @ 60Hz
- Max External Display: QHD @ 60Hz
- Display Pixels: 2560x1440, 2048x1536

General Audio

- Qualcomm Aqstic technology: Qualcomm Aqstic™ audio codec, Qualcomm Aqstic smart speaker amplifier
- Qualcomm® aptX™ audio playback support: aptX, aptX HD

Audio Playback

- PCM, Playback: Up to 384kHz/32bit
- Additional Playback Features: Native DSD support

Qualcomm® AI Engine

- AIE CPU: Octa-core Kryo 468 CPU

- Uplink Technology: Qualcomm® Snapdragon™ Upload+
- Uplink Carrier Aggregation: 2x20 MHz carrier aggregation
- Uplink QAM: Up to 64-QAM
- LTE Speed
- LTE Peak Download Speed: 600 Mbps

Wi-Fi

- Wi-Fi Standards: 802.11ac Wave 2, 802.11a/b/g, 802.11n
- Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz
- MIMO Configuration: 2x2 (2-stream)
- Qualcomm® FastConnect™ Subsystem

Bluetooth Version

- Bluetooth 5.0

GPS Location

- Satellite Systems Support: NavIC, BeiDou, Galileo, GLONASS, GPS, QZSS, SBAS

Security

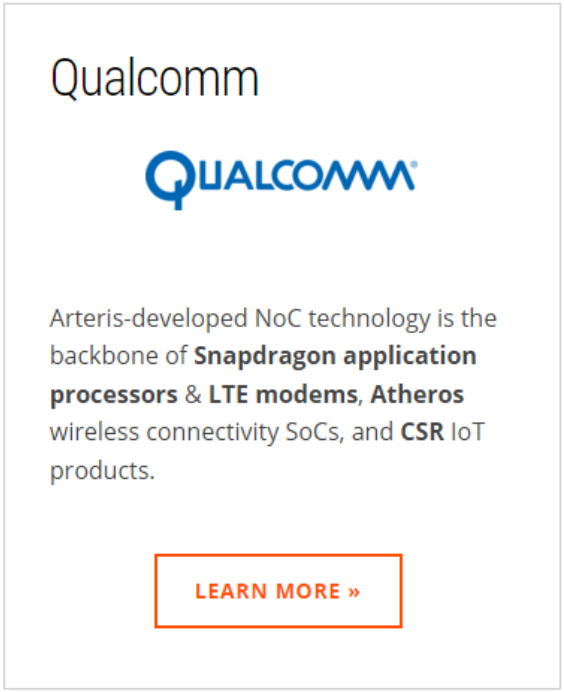
- Qualcomm® Processor Security
- Qualcomm® Content Protection
- Wi-Fi Security: WPA3

U.S. Patent No. 7,366,818 (Radulescu & Goossens)

"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	 https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/prod_brief_qcom_sd7c_gen2.pdf
a network (N; RN) arranged for providing at least one connection between a first and at least one second module (M, S), wherein said modules communicate via a	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Snapdragon SoC included in the Lenovo product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") as a network (N; RN) arranged for providing connections between a first and at least one second module (M, S) in the Snapdragon SoC included in the Lenovo product, wherein said modules communicate via a network on chip, either literally or under the doctrine of equivalents.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
network on chip, and	 https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
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'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	Certain Arteris Technology Assets Acquired by **Kurt Shuler**, on October 31, 2013 Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. ("Qualcomm"), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris. *Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris' Network-on-Chip interconnect IP technology.* ARTERIS IP *K. Charles Janac, President and CEO, **Arteris*** https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team For example, in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets":

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]

11.3.1.1 Transaction Layer

The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:

- A master sends request packets.
- Then, the slave returns response packets.

As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]

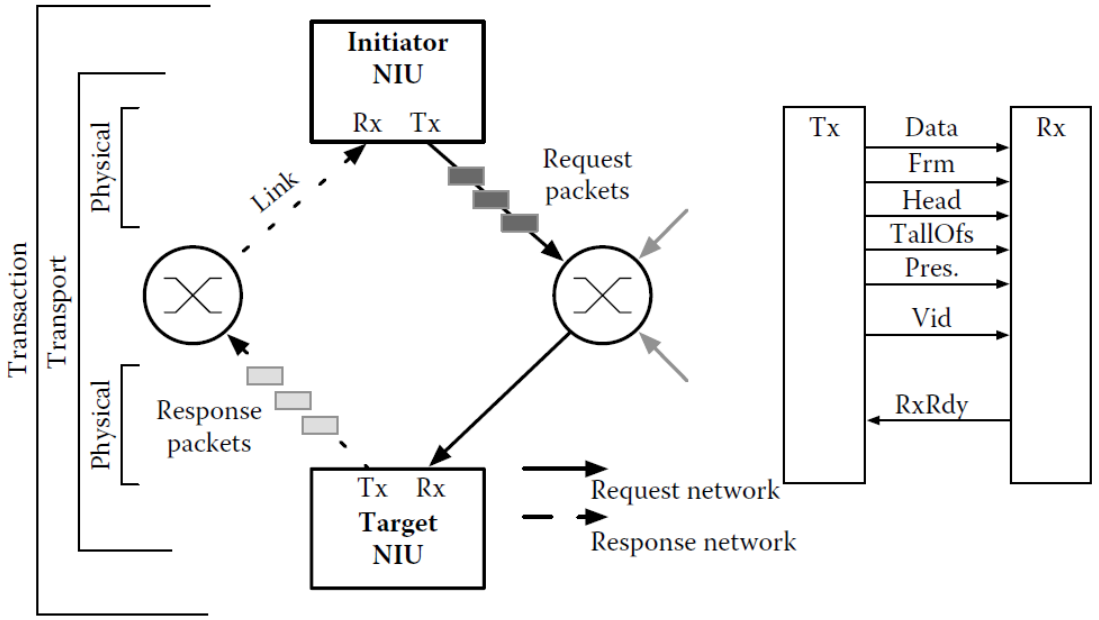


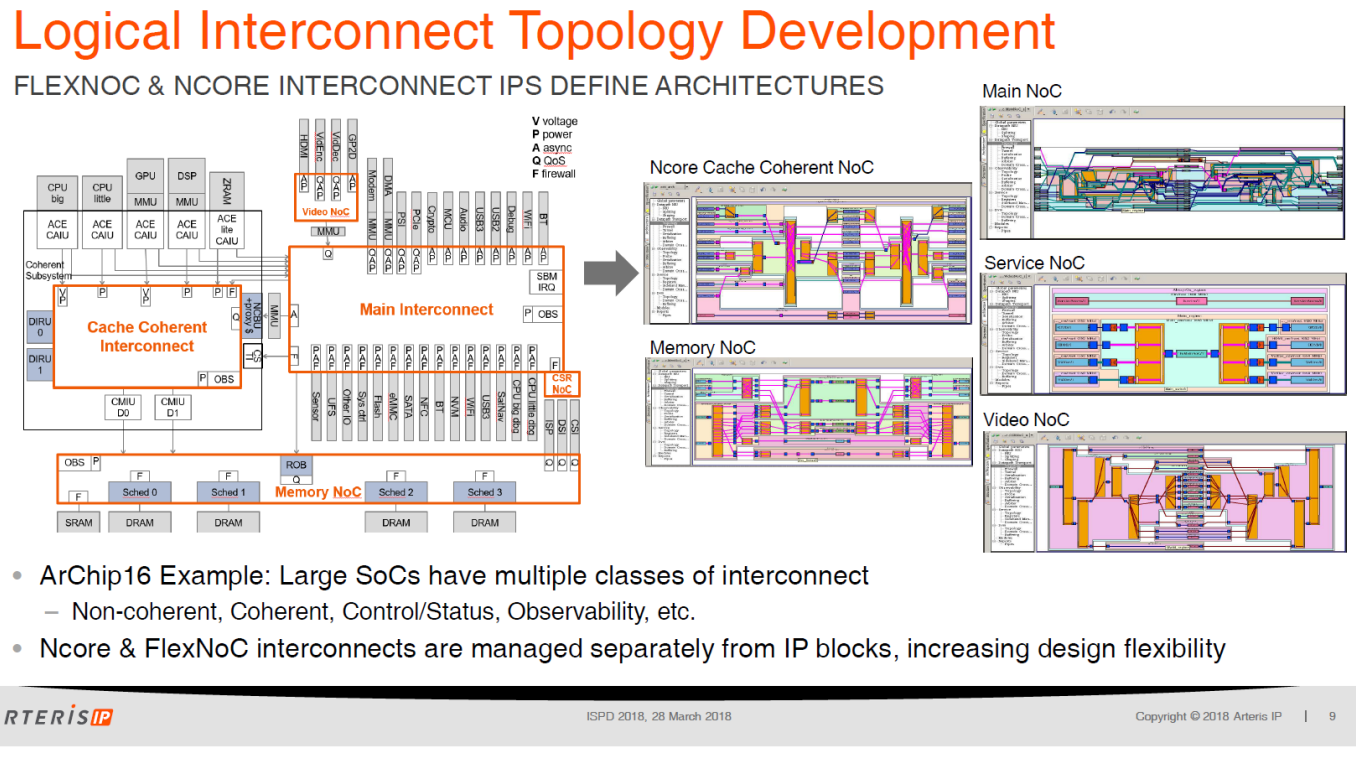
FIGURE 11.1
NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure.").

A large SoC, such as the Snapdragon SoC included in the Lenovo product may include multiple classes of Arteris NoC:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

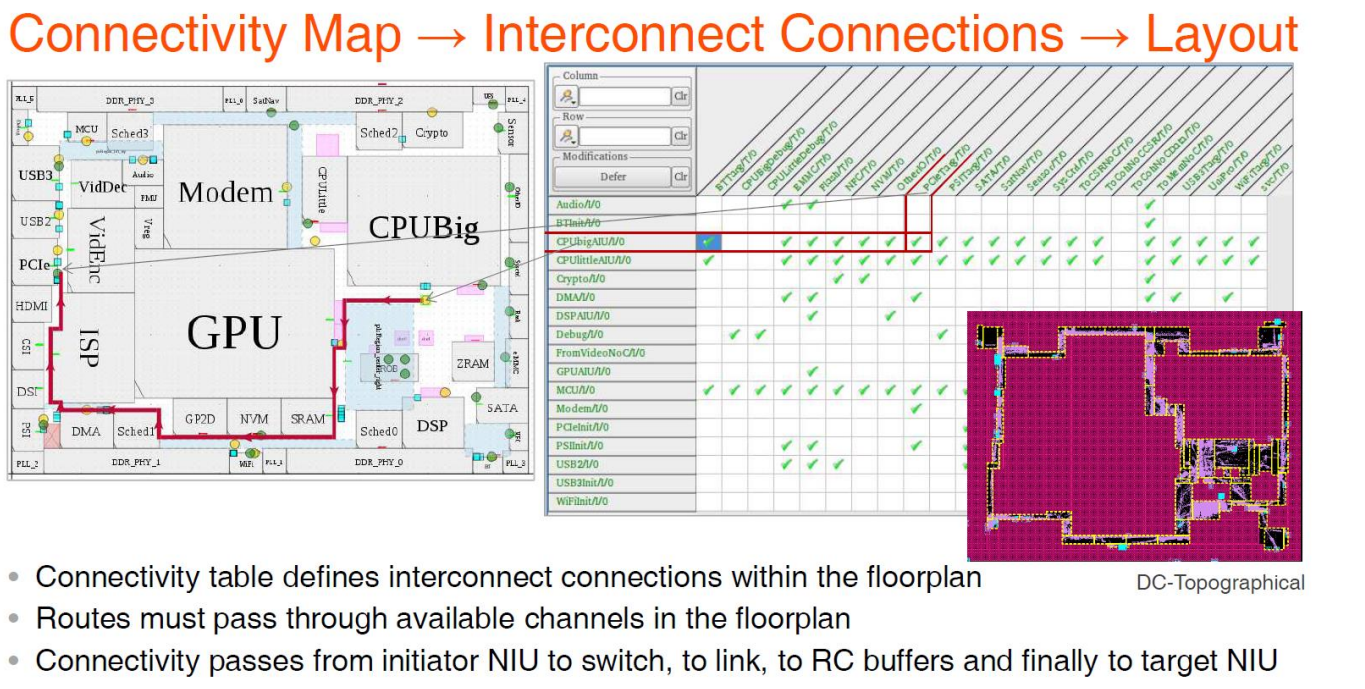
'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]



See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

As a further illustration, connections between modules within the Arteris NoC may be defined by a connectivity table:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.
wherein said connection supports transactions comprising outgoing messages	The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product has a connection that supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module, either literally or under the doctrine of equivalents. For example, in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets":

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
from the first module to the second modules and return messages from the second modules to the first module	***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
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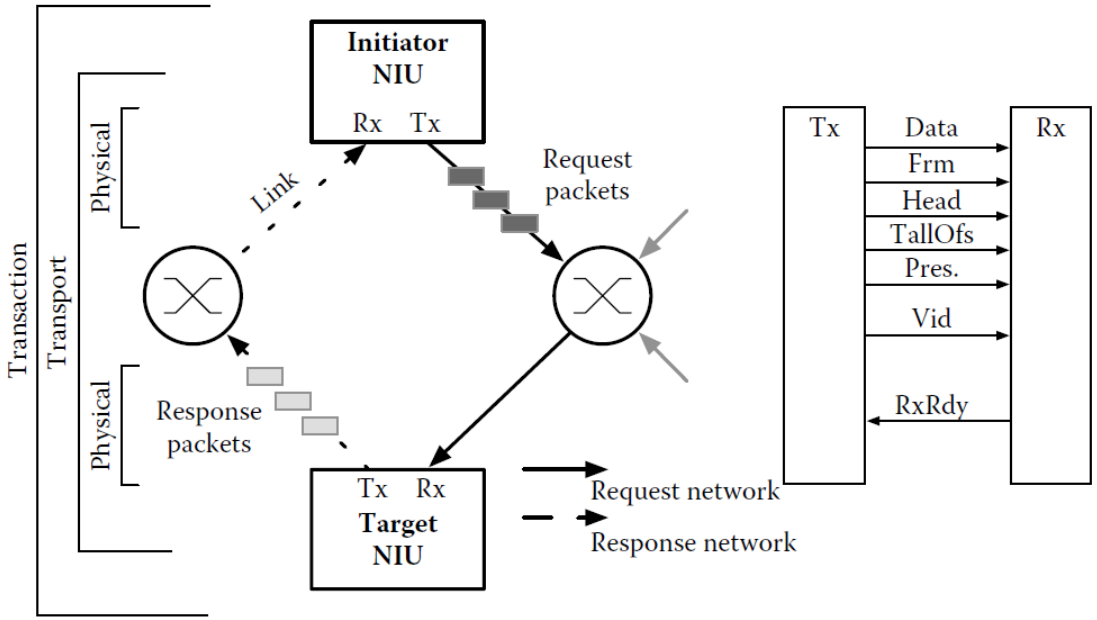
'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.
the integrated circuit comprising at least one dropping means (DM) for dropping	The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product has at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), either literally or under the doctrine of equivalents.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
data exchanged by said first and second module (M, S), and	For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:

Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; **Initiator timeout**
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

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ARTERIS IP + arm

Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.

As a further example, the Arteris NoC includes "packet validity checking" and "transaction timeout" for error resiliency, which may result in data being dropped:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	A. Advanced Data Protection and Reliability for SoC Interconnects Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller. The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent. Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7. As a further example, in the Arteris NoC, "[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC," which may result in data being dropped:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	C. Transaction Timeout Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption. SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.
at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),	The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product has at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN), either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC, the NIUs "are at the boundary of the NoC" and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

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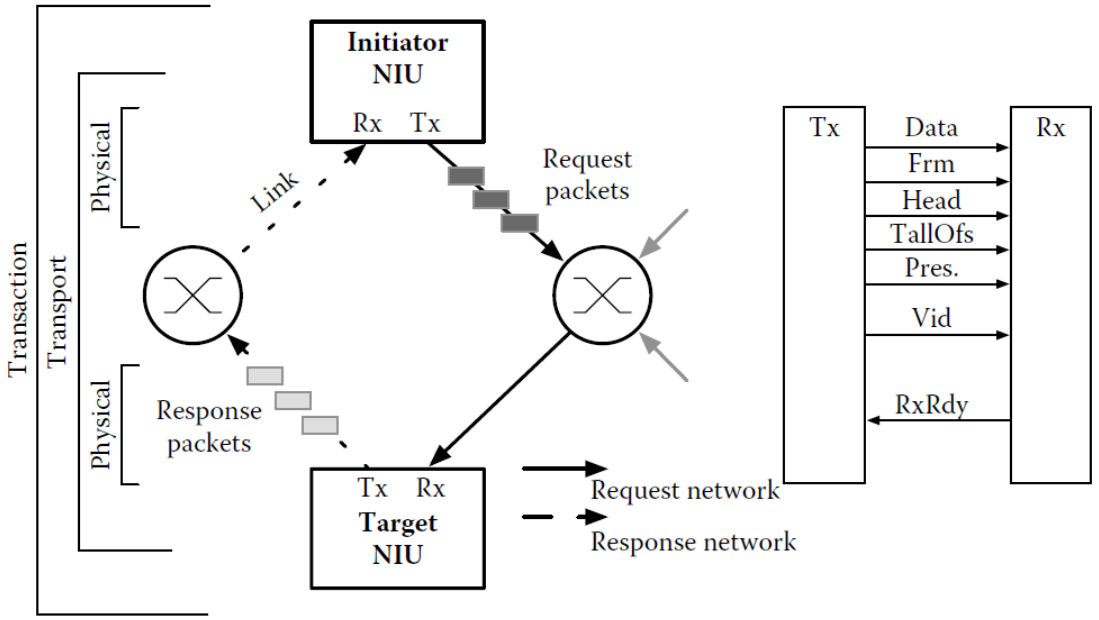

FIGURE 11.1
NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.

The Initiator NIUs are "used to connect a master node to the NoC," and the Target NIUs are "used to connect a slave node to the NoC":

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	11.3.2 Network Interface Units The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated: • **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. In the Arteris NoC "Initiator NIU units…enable connection between an AMBA-AHB master IP and the NoC":

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	11.3.2.1 Initiator NIU Units Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU. A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]

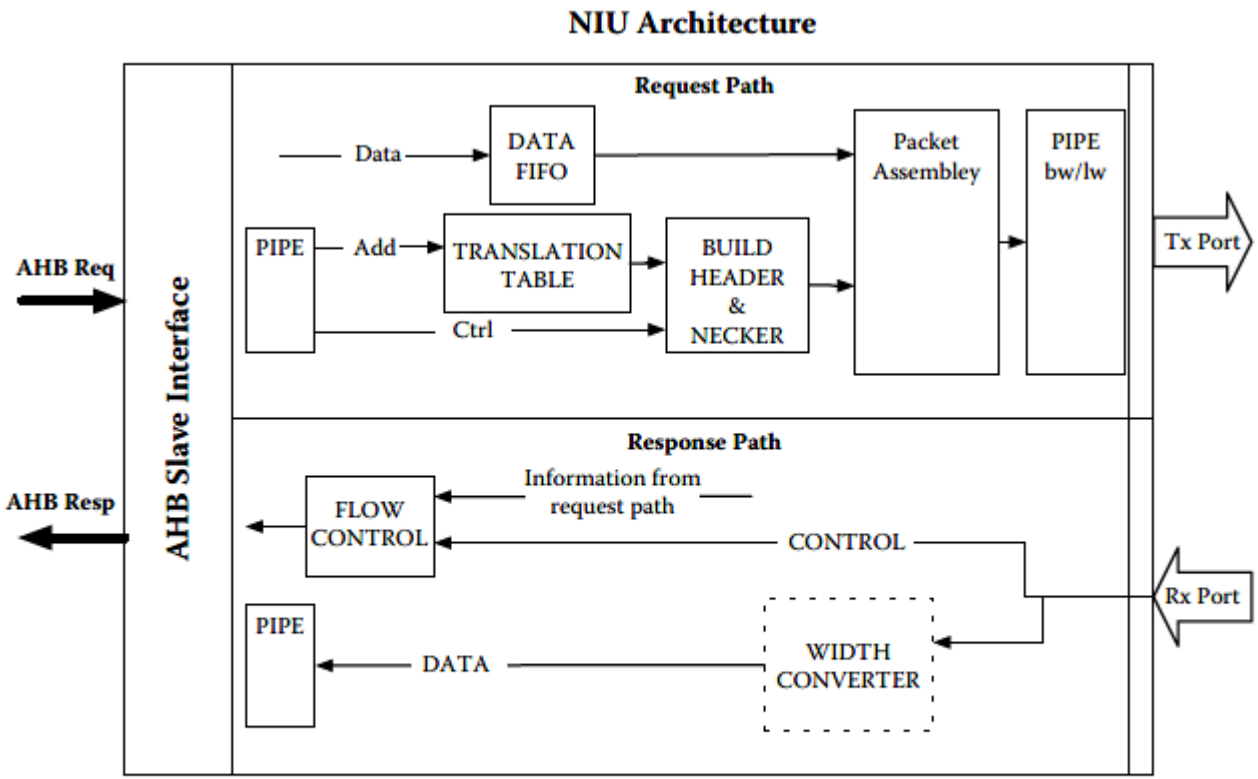

FIGURE 11.4
Network interface unit: Initiator architecture.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.

As further example, "Target NIU units enable connection of a slave IP to the NoC by translating

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets": ***11.3.2.2 Target NIU Units*** Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]

Target NIU Architecture

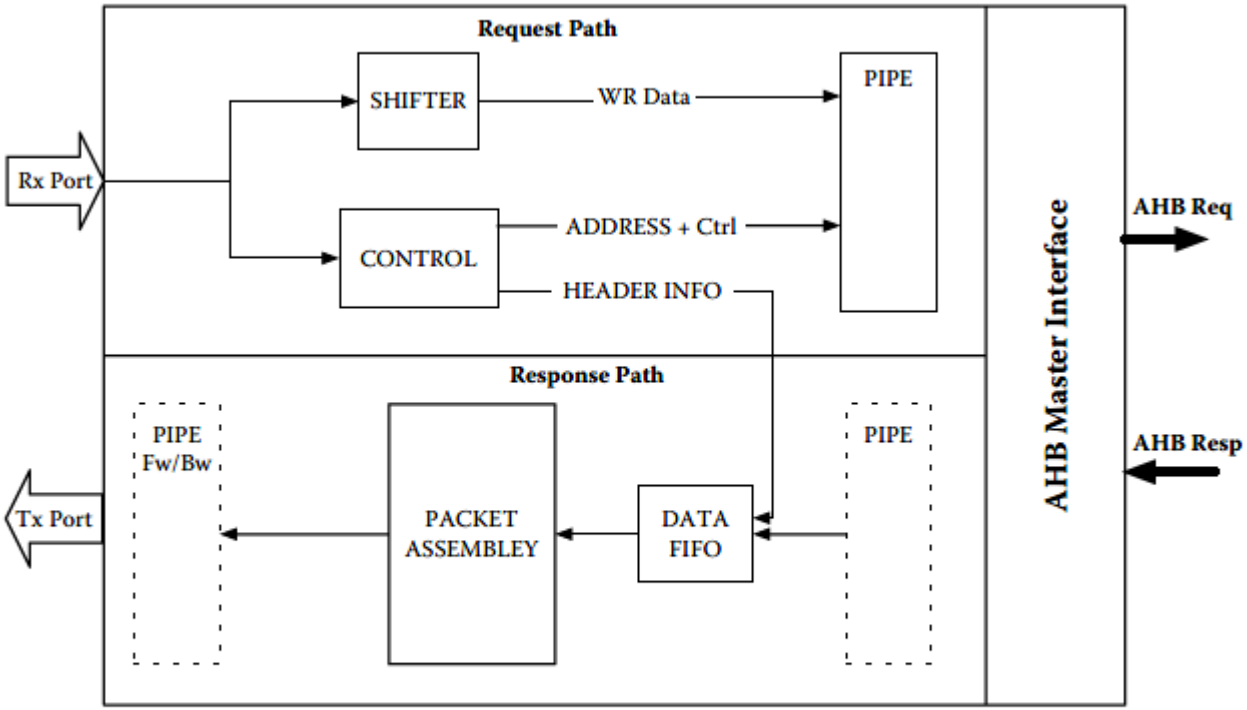

FIGURE 11.5
Network interface unit: Target architecture.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and	The interface means of the Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product comprises a first dropping means (DM) for dropping data, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are "used to connect a master node to the NoC," and the Target NIUs, that are "used to connect a slave node to the NoC": **11.3.2 Network Interface Units** The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated: • **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

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Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; **Initiator timeout**
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

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Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.

As a further example, the Arteris NoC "can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces" and includes "packet validity checking" and "transaction timeout" for error resiliency, which may result in data being dropped:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Lenovo Product Including Snapdragon System on Chip [1]
	A. Advanced Data Protection and Reliability for SoC Interconnects Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller. The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent. Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7. As a further example, in the Arteris NoC, "[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC," which may result in data being dropped:

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	C. Transaction Timeout Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption. SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.
wherein the dropping of data and therefore the transaction completion can be controlled by the interface means.	In the Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product, the transaction completion can be controlled by the interface means, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are "used to connect a master node to the NoC," and the Target NIUs, that are "used to connect a slave node to the NoC": **11.3.2 Network Interface Units** The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:

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	• **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:

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Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; **Initiator timeout**
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

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